ABSTRACT

A technique for forming at least part of an array of a dual bit memory core is disclosed. Initially, a portion of a charge trapping dielectric layer is formed over a substrate and a resist is formed over the portion of the charge trapping dielectric layer. The resist is patterned and a pocket implant is performed at an angle to establish pocket implants within the substrate. A bitline implant is then performed to establish buried bitlines within the substrate. The patterned resist is then removed and the remainder of the charge trapping dielectric layer is formed. A wordline material is formed over the remainder of the charge trapping dielectric layer and patterned to form wordlines that overlie the bitlines. The pocket implants serve to mitigate, among other things, complementary bit disturb (CBD) that can result from semiconductor scaling. As such, semiconductor devices can be made smaller and increased packing densities can be achieved by virtue of the inventive concepts set forth herein.